UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,094	02/01/2005	Atsushi Togawa	09812.0209	8568

22852 7590 12/28/2009

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
BRYANT, DOUGLAS J.	

ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
12/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,094	TOGAWA, ATSUSHI	
	Examiner	Art Unit	
	DOUGLAS BRYANT	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claim language is not clearly understood:

i. As per claim 1, line 6, it is not clearly stated as to what basis is the timing of switching, When or why or how is the timing of the switching working. As per claim1, line 13, it is not clearly indicated as to which OS is the required OS, is the required OS the OS that received the interrupt request or is it the "other" OS? As Per claim 1, line 15-18, it is not clearly stated as to what happens if the time of the next scheduled switch is ***more than*** the maximum allowable delay time from receipt of the interrupt request, does the required OS execute anyway or does it sit idle, or does it require another OS other than the required OS to execute the interrupt request?

ii. Claims 10 and 17 are rejected for similar rejections as claim 1.

iii. Claims 2-9 and 11-16 are rejected for the same reason above because they do not cure the deficiency of 112 2nd issues from their parent claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bollella (Bollella) US Patent Application 2001/0054055 A1, in view of Takeo et al (Takeo) US Patent Application 2002/002538 and in further view of Hitachi Ltd (Hitachi) European Patent Application EP 1162536 A1.

4. As per claim 1, Bollella teaches an information processing apparatus, comprising: a storage section storing a plurality of operating systems (OSs);

a first processor that executes processes of the Oss **(Para 23, lines 2-4)**; and

a process manager that **(Para 47, line 1; multiplexor is the process manager)**:

schedules execution of partitions of the OSs along a time axis **(Para 24, lines 4-7; constant intervals is a time axis)**,

controls the timing of switching between execution of the partitions in accordance with the schedule **(Para 47, lines 1-3; controls when and how long each OS may use shared device)**.

5. Bollella is silent to the teachings wherein the apparatus receives an interrupt request having a maximum time that execution of an interrupt associated with the interrupt request can be delayed from receipt of the interrupt request. requiring an OS other than the OS executing in the current partition to execute the interrupt allowable execution delay time, determines whether the time to a next scheduled switch to the required OS is less than the maximum allowable delay time from receipt of the interrupt request, and when the time to the next scheduled switch is less than the maximum allowable delay time from receipt of the interrupt request, causes the required OS to execute the interrupt request at the time of the next scheduled switching.

6. However Takeo teaches an apparatus that receives an interrupt request having a maximum time that execution of an interrupt associated with the interrupt request can be delayed from receipt of the interrupt request **(Para 141, lines 1-5; it's understood that anytime before an absolute start time is the maximum delay time).**

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Takeo into the methods of Bollella to send a request with an absolute start time letting the system know the maximum delay time before interrupt request has to be processed in order to maintain it deadline. This modification would have been obvious because one of ordinary skill in the art would want to know the maximum delay time for a request in order to avoid processing errors caused by exceeding wait times during an interrupt request.

8. Bollella and Takeo are both silent to the teachings wherein requiring an OS other than the OS executing in the current partition to execute the interrupt allowable execution delay and determines whether the time to a next scheduled switch to the required OS is less than the maximum allowable delay time from receipt of the interrupt request and when the time to the next scheduled switch is less than the maximum allowable delay time from receipt of the interrupt request, causes the required OS to execute the interrupt request at the time of the next scheduled switching

9. However Hitachi teaches requiring an OS other than the OS executing in the current partition to execute the interrupt allowable execution delay time **(Col 9, lines 25-31; it is understood that if there is not enough time left in the slot of OS-B to handle the procedure, that OS-A becomes the required OS)**,

determines whether the time to a next scheduled switch to the required OS is less than the maximum allowable delay time from receipt of the interrupt request **(Col 9, lines 25-30; judging by referring to the predefined execution time for OS-B determines if the schedule switch is less than the max delay time)**, and

when the time to the next scheduled switch is less than the maximum allowable delay time from receipt of the interrupt request, causes the required OS to execute the interrupt request at the time of the next scheduled switching **(Col 8, lines 25-31; it is understood that the procedure goes to OS-A means that the time was less than the max delay time allowed)**.

10. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Hitachi into the methods of Bollella to determine the maximum delay time before interrupt request has to be processed in order to maintain it deadline. This modification would have been obvious because one of ordinary skill in the art would want to know the maximum delay time for a request in order to avoid processing errors caused by exceeding wait times during an interrupt request.

11. As per claim 2, Bollella teaches the information processing apparatus according to claim 1, wherein the process manager is configured to interrupt execution of the partitions at the time of an earliest scheduled switch after receiving occurrence of the interrupt request **(Para 61, lines 5-6 {at the end of each interval is the earliest scheduled switch})**.

12. As per claim 3, Hitachi teaches he information processing apparatus according to claim 1, wherein the process manager is further configured to suspended execution of the partitions to execute the interrupt process, when it is determined that the time to the next switch is longer than the maximum allowable delay time from the occurrence of the interrupt request **(Col 9, lines 3-44; it is understood that if the time comes for OS-B and it stays idle, the task is suspended until OS-A slot comes back around).**

13. As per to claim 4, Bollella teaches the information processing apparatus according to claim 1, further comprising:

a second processor that executes the processes of the OSs in parallel with the first processor, wherein the process manager is further configured to **(Para 64, lines 2-6 {multiplexing….executing the GPOS for contiguous time units & RTK for contiguous})**:

schedule execution of the partitions along the time axis as to the first and second processors such that the first and second processors switch between execution of the partitions in accordance with the schedule **Para 24, line 6 {its execution at precise constant intervals [precise intervals is schedule on a time axis})**,

select a schedule corresponding to the first processor or to the second processor **(Para 47, lines 4-6; multiplexor precisely allocates (schedules) execution time…..to each OS),** and

interrupt execution of the partitions by the first processor or the second processor at the time of a scheduled switch between execution of the partitions contained in the selected schedule**(Para 47, lines 1-3; the multiplexor….. controls when and how long each OS may use a shared device).**

14. As per claim 5, Bollella teaches the information processing apparatus according to claim 4, wherein the process manager is configured to:

select a schedule having the earliest scheduled switch between execution of the partitions after receiving the interrupt request, and interrupt execution of the partitions at the time of the earliest scheduled switch**(Para 48, lines 8-12 {it must logically execute all interrupts.....until it has allocated the desired units... (e.g. CPU cycle allotment) }).**

15. As per claim 6, Bollella teaches the information processing apparatus according to claim 1, wherein the process manager is further configured to:

receive a second interrupt request having a minimum allowable execution delay time **(Para. 62, lines 23-25 {Loop continues until…..another marker occurs})**, and

interrupt execution of the partitions at the time of a scheduled switch between execution of the partitions that occurs after the minimum allowable delay time from receipt of the second interrupt request has elapsed **(Para. 62, line 25 {control passes to terminate RTK})**.

16. As per claim 7, Bollella teaches the information processing apparatus according to claim 1, wherein the process manager is further configured to:

receive a second interrupt request that is executable during execution of a specific partition, determine, based on the schedule, when the specific partition will be executed, and when the specific partition is being executed, interrupt execution of the specific partition to execute the second interrupt request **(Para. 62, lines 26-29 {RTK is executing, continual test for another marker…if so a test is made to see if it is time to execute GPOS. If so controls pass to GPOS})**

17. As per claim 8, Bollella teaches the information processing apparatus according to claim 1, further comprising:

a second processor that executes the processes of the OSs in parallel with the first processor **(Para 22, lines1-5 {partition the central processor……first machine GPOS….second machine RTK})**, and

first and second partition switching modules for respectively controlling the processors to switch between execution of the partitions, wherein the process manager is further configured to control the first and second partition switching modules to cause the processors to execute the partitions in accordance with the schedule**(Para 47, lines 1-6 {the multiplexor….. controls when and how long each OS may use a shared device} (Para 61, lines 5-6 {at the end of each interval is the earliest scheduled switch}).**

18. As per claim 9, Bollella teaches the information processing apparatus according to claim 8, further comprising:

a memory storing reservation queues of entries containing information about received interrupt requests **(Para 62, lines 31-32 { state is saved for the RTK and GPOS})**,

the queues being grouped based on sources from which the interrupt requests originated wherein the first and second partition switching modules are configured to select, from the reservation queues and based on the grouping, entries corresponding to interrupt requests originating from sources which can be accommodated by the processors, respectively **(Para 72, lines 9-13 {interrupt vector table contains information….permission values and type information}; Para 73, lines 9-12 {global descriptor table uses the values….to identify code currently executing….decisions based on that determination}).**

19. As per claim 10 and 17, they are rejected on the same rationale as claim 1.

20. As per claim 11, it is rejected on the same rationale as claim 2.

21. As per claim 12, it is rejected on the same rationale as claim 3.

22. As per claim13, Bollella teaches the method according to claim 10, further comprising including:

scheduling, by the processor, execution of the partitions along a time axis as to a plurality of processors that execute the partitions of the Oss **(Para 22, lines1-5 {partition the central processor……first machine GPOS….second machine RTK} Para 24, line 6 {its execution at precise constant intervals [precise intervals is schedule on a time axis})**,

of such that the processors switch between execution of the partitions in accordance with the schedule, selecting, by the processor, a schedule corresponding to one of the plurality of processors, and interrupting, by the processor, execution of the partitions by the processor corresponding to the selected schedule to execute the interrupt processing request **(Para 47, lines 1-6 {the multiplexor….. controls when and how long each OS may use a shared device}).**

23. As per claim 14, Bollella teaches the method according to claim 13, wherein interrupting execution includes selecting, by the processor, in which a schedule having an earliest scheduled switch between execution of the partitions after receipt of the interrupt request, and executing, by the processor, the interrupt processing request at the time of the earliest scheduled switch **(Para 48, lines 8-12 {it must logically execute all interrupts.....until it has allocated the desired units...CPU cycle allotment}).**

24. As per claim 15, Bollella teaches the method according to claim 10, further comprising: receiving, by the processor, a second processing interrupt request having a minimum allowable execution delay time **(Para. 62, lines 23-25 {Loop continues until…..another marker occurs})**,

scheduling, by the processor, execution of the second interrupt processing request at the time of a scheduled switch between execution of the partitions that occurs after the minimum allowable delay time has elapsed **(Para. 62, line 25 {control passes to terminate RTK})**.

25. As per claim 16, Bollella teaches the method according to claim 10, further comprising: receiving, by the processor, a second interrupt processing request that is executable during execution of a specific partition, determining, by the processor and based on the schedule, when the specific partition will be executed, and when the specific partition is being executed, interrupting, by the processor, execution of the specific partition to execute the second interrupt processing request **(Para. 62, lines 26-29 {RTK is executing, continual test for another marker…if so a test is made to see if it is time to execute GPOS. If so controls pass to GPOS})**.

Response to Arguments

26. Applicant's arguments with respect to claims 1-16 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DOUGLAS BRYANT whose telephone number is (571)270-7707. The examiner can normally be reached on M-F 8:00-5:00pm Est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-ai can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/D. B./
Examiner, Art Unit 2195